METAL-OXIDE-SEMICONDUCTOR DEVICE
HAVING IMPROVED PERFORMANCE AND RELIABILITY

Field of the Invention

The present invention relates generally to semiconductor devices, and more particularly

5   relates to techniques for forming an MOS device having improved reliability without significantly

impacting high-frequency performance.

Background of the Invention

Power MOS devices, including laterally diffused metal-oxide-semiconductor (LDMOS)

devices, are employed in a variety of applications, such as, for example, power amplifiers in wireless

10   communications systems. In a conventional LDMOS device, hot-carrier injection (HCI) effects,

current crowding in a lightly-doped drain (LDD) region and/or electric field distribution are some

of the phenomena which are known to undesirably affect the performance and reliability of the

device.

HCI in an MOS device generally results from heating and subsequent injection of carriers

15   into the gate oxide of the device, which results in a localized and nonuniform buildup of interface

states and oxide charges near and underneath a gate of the device. As is well known in the art, the

buildup of interface states, which are typically defined as trapped charges in an interface between

an upper surface of the silicon substrate and an oxide layer formed on the substrate, generally results

from a high electric field distribution proximate the silicon/oxide interface. This phenomenon can

20   produce variations in certain characteristics of the MOS device, including threshold voltage,

transconductance, drain current, etc., thus undesirably affecting the performance and reliability of

the device. It is well known that HCI is a strong function of the internal electric field distributions

at the silicon/oxide interface of the MOS device.

In order to reduce HCI effects somewhat in an LDMOS device, it is known that the source

25   metal, which provides electrical connection to the source region of the device, may be extended over

the gate so as to form a shielding structure. The source contact may thus be used to form a Faraday

shield over the gate, which helps reduce the high electric field concentration near the corners of the

gate. However, while the Faraday shield may provide a limited reduction in HCI effects, it typically does not reduce current crowding and confinement in the LDD region of the device. It is this current crowding and confinement, particularly near an edge of the gate and in the thin LDD region near a silicon/oxide interface in the device, which primarily contributes to HCI.

5   As an added drawback, the conventional shielding structure prevents full gate metalization, which is one known method for dramatically reducing the resistance Rg of the gate, thus limiting the high-frequency performance of the LDMOS device. Since the output gain of the MOS device is inversely proportional to the gate resistance of the device, increasing the gate resistance results in a decrease in the output gain of the device, which is particularly undesirable in an amplifier

10   application.

There exists a need, therefore, for an MOS device capable of improved performance and reliability that does not suffer from at least the above-noted deficiencies typically affecting conventional MOS devices. Furthermore, it would be desirable if such an MOS device was fully · compatible with a CMOS process technology.

15   **Summary of the Invention**

The present invention provides techniques for reducing undesirable effects including HCI, current crowding, and/or high electric field distribution in an MOS device, thereby improving performance and reliability without undesirably affecting high-frequency performance of the device. Moreover, the techniques of the present invention can be used to fabricate an integrated circuit (IC)

20   device, for example, an LDMOS device, using conventional CMOS compatible process technology. Consequently, the cost of manufacturing the IC device is not significantly increased.

In accordance with one aspect of the invention, an MOS device includes a semiconductor layer comprising a substrate of a first conductivity type and a second layer of a second conductivity type formed on at least a portion of the substrate. First and second source/drain regions of the second

25   conductivity type are formed in the second layer proximate an upper surface of the second layer, the second layer being spaced laterally from the first source/drain region. A gate is formed above the second layer proximate the upper surface of the second layer and at least partially between the first

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and second source/drain regions. The MOS device further includes at least one electrically conductive trench formed in the second layer between the gate and the second source/drain region, the trench being formed proximate the upper surface of the semiconductor layer and extending substantially vertically through the second layer to the substrate.

5   The at least one trench is preferably configured such that as a voltage at the second source/drain region increases, a depletion region spreads outward from the trench so as to substantially fill a region proximate the trench. The MOS device provides reduced HCI effects, reduced current crowding and/or a reduced peak electric field near the gate, particularly in an area proximate the upper surface of the semiconductor layer, without substantially degrading high-

10   frequency performance. Furthermore, the MOS device is substantially compatible with a CMOS process technology.

        These and other features and advantages of the present invention will become apparent from the following detailed description of illustrative embodiments thereof, which is to be read in connection with the accompanying drawings.

15   **Brief Description of the Drawings**

        FIG. 1 is a cross-sectional view illustrating at least a portion of an LDMOS device in which the techniques of the present invention can be implemented.

        FIG. 2 is a cross-sectional view depicting at least a portion of an exemplary LDMOS device, formed in accordance with an illustrative embodiment of the present invention.

20   FIGS. 3A through 3D are cross-sectional views depicting steps in an illustrative semiconductor fabrication process which may be used in forming the exemplary LDMOS device shown in FIG. 2.

Detailed Description of the Preferred Embodiments

        The present invention will be described herein in the context of an illustrative CMOS

25   integrated circuit fabrication technology suitable for forming discrete RF LDMOS transistors, as well as other devices and/or circuits. It should be appreciated, however, that the present invention is not

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limited to the fabrication of this or any particular device or circuit. Rather, the invention is more generally applicable to any MOS device in which it is desirable to alleviate effects including HCI, current crowding and/or high electric field distribution, thereby improving the performance and reliability of the device without significantly affecting high-frequency performance in the device.

5   Although implementations of the present invention are described herein with specific reference to an LDMOS device, it is to be appreciated that the techniques of the present invention are similarly applicable to other devices, such as, but not limited to, a vertical diffused MOS (DMOS) device, an extended drain MOS device, etc., with or without modifications thereto, as will be understood by those skilled in the art. Furthermore, although the invention will be described herein in the context of a p-channel MOS device, it is well understood by those skilled in the art that an n-channel MOS device could be formed by simply substituting opposite polarities to those given for the p-channel embodiment, and that the techniques and advantages of the present invention will similarly apply to the alternative embodiment.

It is to be understood that the various layers and/or regions shown in the accompanying figures may not be drawn to scale. Furthermore, one or more semiconductor layers of a type commonly used in such integrated circuit structures may not be explicitly shown in a given figure for ease of explanation. This does not imply that the semiconductor layer(s) not explicitly shown are omitted in the actual integrated circuit device.

FIG. 1 illustrates a cross-sectional view of at least a portion of a semiconductor wafer 100 that can be modified to implement the techniques of the invention. The wafer 100 includes an LDMOS device formed on a substrate 102. The LDMOS device includes a source region 106 and a drain region 108 formed in an epitaxial layer 104 of the wafer 100. The LDMOS device further includes a gate 110 formed above a channel region 112 of the device. The channel region 112 is at least partially formed between the source and drain regions. A drift region is generally formed in the epitaxial layer 104 of the LDMOS device which may comprise a first LDD region (ldd1) 114 and a second LDD region (ldd2) 116 formed between the channel region 112 and drain region 108. The source region 106 in the LDMOS device may include a body region (p-body) 118 formed in the epitaxial layer 104 adjacent to the source region 106 and extending laterally opposite the channel

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region 112. An oxide layer 124 is generally formed on an upper surface of the wafer 100 to electrically isolate the source, drain and gate areas of the device as well as to protect the device.

The LDMOS device further includes a drain contact 120 and a source contact 122, each of which may be formed in or through the oxide layer 124 and electrically connected to the drain region

5   108 and source region 106, respectively. Electrical contact to the source region 106 may also be made from a bottom of the substrate 102 via one or more trench sinkers 128 formed through the epitaxial layer 104 which provide a low-resistance (e.g., less than about 1 ohm per square) electrical path between the source region 106 and the substrate 102. A gate contact (not shown) is also included for providing an electrical connection to the gate 110.

10   Due at least in part to the relatively high electric field concentration near the corners of the gate 110 and the close relative proximity of the gate to an interface between the upper surface of the silicon and the oxide layer 124, HCI often occurs at the silicon/oxide interface near the first LDD region 114 immediately proximate the edge of the gate 110. In order to reduce HCI in the LDMOS device, the source contact 122 may be extended over the gate 110 and ending proximate an upper

15   surface of the wafer 100 between the gate and drain region 108 so as to form a shielding structure. The source contact 122 thus forms a Faraday shield over the gate 110 which helps distribute the high electric field concentration near the corners of the gate. Although not shown, a separate shielding structure, referred to herein as a dummy gate, may alternatively be formed in close relative proximity to the gate 110, between the gate 110 and drain region 108 and in close proximity (e.g., 200

20   nanometers (nm)) to the upper surface of the wafer 100. If used, the dummy gate is electrically connected (e.g., strapped) to the source region 106.

While employing a shielding structure (e.g., Faraday shield or dummy gate) may help reduce HCI degradation at a silicon/oxide interface between the oxide layer 124 and an upper surface of the epitaxial layer 104, HCI degradation will generally increase at the silicon/oxide interface near the

25   second LDD region 116 immediately proximate an edge of the shielding structure. HCI degradation can be further reduced by lowering the doping concentration of at least the first LDD region 114. However, this will undesirably result in an increase in the on-resistance associated with the device.

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Thus, in a conventional LDMOS device, there is often a trade-off which exists between on-resistance and HCI effects in the device.

FIG. 2 illustrates a cross-sectional view of at least a portion of a semiconductor wafer 200 in which the techniques of the present invention are implemented. As previously stated, the various
5   layers and/or regions shown in the figure may not be drawn to scale and certain commonly used semiconductor layers may have been omitted for ease of explanation. The wafer 200 includes an exemplary LDMOS device formed on a semiconductor substrate 202. The substrate 202 is commonly formed of single-crystal silicon, although alternative materials may be used, such as, but not limited to, germanium (Ge), gallium arsenide (GaAs), etc. Additionally, the substrate 202 may
10   have been modified by adding an impurity or dopant, such as by a diffusion or implant step, to change the conductivity of the material (e.g., n-type or p-type). In a preferred embodiment of the invention, the substrate 202 is of p-type conductivity, and hence may be referred to as a p-substrate.

The term "semiconductor layer" as may be used herein refers to any semiconductor material upon which and/or in which other materials may be formed. The semiconductor layer may comprise
15   a single layer, such as, for example, the substrate 202, or it may comprise multiple layers, such as, for example, the substrate 202 and an epitaxial layer 204. In a preferred embodiment of the invention, the epitaxial layer 204 is of n-type conductivity. The semiconductor wafer 200 comprises the substrate 202, with or without the epitaxial layer 204, and preferably includes one or more other semiconductor layers formed on the substrate. The term "wafer" is often used interchangeably with
20   the term "silicon body," since silicon is typically employed as the semiconductor material comprising the wafer. It should be appreciated that although the present invention is illustrated herein using a portion of a semiconductor wafer, the term "wafer" may include a multiple-die wafer, a single-die wafer, or any other arrangement of semiconductor material on or in which a circuit element may be formed.

25   The exemplary LDMOS device includes a source region 206 and a drain region 208 formed in the epitaxial layer 204 of the wafer 200, such as by an implant or diffusion process. The source and drain regions are preferably doped, such as by an implant process, with an impurity (e.g., boron, phosphorus, etc.) of a known concentration level to selectively change the conductivity of the

material as desired. Preferably, the source and drain regions 206, 208 have a conductivity type associated therewith which is opposite a conductivity type of the substrate 202, so that active regions can be formed in the device. In a preferred embodiment of the invention, the source and drain regions 206, 208 are of n-type conductivity. A low-resistance (e.g., less than about ten ohms per

5 square) electrical path between the source region 206 and the substrate 202 may be provided by forming one or more trench sinkers 226 through the epitaxial layer 204 of the wafer 200. The trench sinkers 226 may be formed in a conventional manner, such as, for example, by forming openings in the epitaxial layer 204 (e.g., by photolithographic patterning and etching) to expose the substrate 202, and filling the openings with an electrically conductive material, as will be understood by those

10 skilled in the art. In a preferred embodiment of the invention, the trench sinkers 226 are of p-type conductivity.

It is to be appreciated that, in the case of a simple MOS device, because the MOS device is symmetrical in nature, and thus bidirectional, the assignment of source and drain designations in the MOS device is essentially arbitrary. Therefore, the source and drain regions may be referred to

15 generally as first and second source/drain regions, respectively, where "source/drain" in this context denotes a source region or a drain region. In an LDMOS device, which is generally not bidirectional, such source and drain designations may not be arbitrarily assigned.

The exemplary LDMOS device includes an body region 216 formed in the epitaxial layer 204, such as by a conventional implant and diffusion process. The body region 216 is preferably

20 formed adjacent to the source region 206 and extends laterally in a direction opposite the drain region 208. The body region 216 is preferably doped, such as by a conventional implant step, with an impurity of a known concentration level to selectively change the conductivity of the material as desired. Preferably, the body region 216 has a conductivity type associated therewith which is opposite a conductivity type of the source region 206. In a preferred embodiment of the invention,

25 the body region 216 is of p-type conductivity, and hence may be referred to as a p-body.

A channel region 214 is formed proximate an upper surface of the exemplary LDMOS device, just beneath an interface between the epitaxial layer 204 and an insulating layer 212, which in a preferred embodiment is formed of an oxide (e.g., silicon dioxide (SiO_2)), although other

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suitable insulating materials may be used (e.g., silicon nitride). Since the epitaxial layer 204 often comprises silicon, this interface may be referred to as a silicon/oxide interface. The channel region 214 is formed at least partially below and adjacent to the source region 206 in the LDMOS device. The channel region 214 may be formed of a material having the same conductivity type as the

5   substrate, preferably p-type in the exemplary device, and may therefore be referred to as a p-channel.

The exemplary LDMOS device further includes a gate 210 formed above at least a portion of the channel region 214 and proximate the silicon/oxide interface of the wafer 200. The gate may comprise, for example, polysilicon material, although alternative suitable materials (e.g., metal) may be similarly employed. The gate 210 is electrically isolated from an active area of the wafer via an

10   insulating layer 212. Since the insulating layer under the gate 210 preferably comprises an oxide (e.g., silicon dioxide), this insulating layer 212 may be referred to herein as gate oxide.

A shielding electrode 218, which may be referred to herein as a dummy gate, is preferably formed in the exemplary LDMOS device between the gate 210 and the drain region 208. The dummy gate 218, which may comprise, for example, polysilicon, is spaced laterally from the gate

15   210 and preferably substantially non-overlapping relative to the gate. Although not shown, the dummy gate 218 in the exemplary LDMOS device, when used, is preferably electrically connected (e.g., strapped) to the source region 206, such as by forming a conductive layer (e.g., aluminum, gold, etc.) between the dummy gate and the source region. Like the gate 210, the dummy gate 218 is preferably formed on the insulating layer 212 for electrically isolating the dummy gate from an

20   active region of the wafer. As previously explained, the dummy gate 218 beneficially reduces HCI proximate the silicon/oxide interface in the vicinity of the corners of the gate 210. A dummy gate suitable for use in conjunction with the present invention can be found, for example, in a related U.S. application serial number 10/623,983 entitled "Shielding Structure for Use in a Metal-Oxide-Semiconductor Device," filed on July 15, 2003, which is incorporated by reference herein.

25   In a preferred embodiment of the invention, the dummy gate 218 is formed concurrently with the gate 210 in the same processing step. In this manner, the dummy gate 218 is preferably self-aligned to the gate 210. The thickness of the insulating layer 212 (e.g., silicon dioxide) beneath the gate 210 and dummy gate 218 may be substantially the same. Thus, like the gate 210, the dummy

gate 218 is preferably formed in close relative proximity (e.g., 200 nanometers (nm)) to the silicon/oxide interface of the wafer 200. It is to be appreciated, however, that the relative thicknesses of the insulating layer 212 under the gate 210 and dummy gate 218 need not be the same. Furthermore, although the size and shape of the dummy gate 218 relative to the gate 210 may be

5   substantially the same, the configuration of the gate and/or dummy gate are not limited to the precise size or shape shown, but may be formed in alternative configurations, as will be understood by those skilled in the art.

A source contact 222 and a drain contact 224 may be formed on an upper surface of the wafer 200, such as, for example, by conventional photolithographic patterning and etching, for providing

10   an electrical connection to the source region 206 and drain region 208, respectively, as will be understood by those skilled in the art. The source and drain contacts may comprise a metal, such as, for example, aluminum or gold. Connection to the source region 206 may also be made through a bottom surface of the substrate since the trench sinkers 226 provide a relatively low-resistance electrical path between the source region 206 and the substrate 202, as previously explained. A gate

15   contact (not shown) may also be formed on the upper surface of the wafer 200, or in an alternative location, for providing an electrical connection to the gate 210.

An important aspect of the present invention is the formation of one or more electrically conductive trenches 220 in the epitaxial layer 204 of the LDMOS device, between the channel region 214 and drain region 208. A given trench 220 may comprise a groove (e.g., v-groove), diffused

20   sinker, or an alternative structure for providing a low-resistance electrical path between the upper surface of the wafer and the substrate 202. Although a single trench may be used, in a preferred embodiment of the invention a plurality of trenches 220 are utilized, each of the trenches preferably extending substantially vertically through the epitaxial layer 204, between the upper surface of the wafer 200 and the substrate 202.

25   The trenches 220 may be formed in a conventional manner, such as, for example, by forming openings or v-grooves in the epitaxial layer 204 (e.g., by photolithographic patterning and etching) to expose the substrate 202, and filling the trenches with an electrically conductive material (e.g., doped polysilicon, metal, silicide, etc.), as will be understood by those skilled in the art.

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Alternatively, the trenches 220 may comprise diffused sinkers, which may be formed in a conventional manner, for example, by doping the surface of the silicon with a heavy impurity predeposition (e.g., boron) or implanting a very high dose ion implant, which is then driven at a high temperature down to the substrate. In essence, since the trenches are electrically connected to the

5   substrate, which like the source region 206 is typically at ground potential, the addition of the trenches 220 advantageously extends the concept and associated benefits of the dummy gate 218 deeper into the epitaxial layer of the device.

The trenches 220 reshape a depletion layer formed in the device in order to protect a region proximate the gate 210 from experiencing a high electric field concentration. This is accomplished,

10   in at least one aspect, by configuring the trenches 220 so as to control a spread of the depletion layer and/or a distribution of an electric field in the device. Therefore, in accordance with one aspect of the invention, the trenches 220 are preferably formed in the epitaxial layer 204 such that as a voltage at the drain region 208 increases, the depletion layer spreads from the trenches to substantially fill a region between the trenches. In this manner, the region between the drain region 208 and gate 210

15   substantially pinches off, thereby reducing the current concentration, and thus the electric field concentration, proximate the gate. In accordance with another aspect of the invention, trenches may also be placed around a periphery of an end of the drain region 208 in order to effectively limit the total drain area, and thus limit a gate-to-drain capacitance of the device. Reducing the gate-to-drain capacitance advantageously improves the high-frequency performance of the device.

20   Traditionally, the current density, and thus the electric field concentration, will be significantly higher along the channel region 214 near the gate 210, particularly where the channel region curves, thereby increasing the likelihood that HCI will occur. The trenches 220 may beneficially control a curvature of the channel region 214, in at least one aspect, by controlling the spread of the depletion layer and the distribution of the electric field proximate the gate 210 so as

25   to reduce HCI effects. Conventionally, the shaping of the channel region and depletion layer is controlled by the LDD regions (e.g., 114 and 116 shown in FIG. 1). These LDD regions are typically formed as very shallow (e.g., in a range from about 0.05 micron to about 0.5 micron) implant regions in the epitaxial layer proximate the silicon/oxide interface. Since the bulk of the current in the

device will flow through the LDD regions, the electric field will inherently be concentrated near the silicon/oxide interface, thus increasing the likelihood of HCI.

The addition of the trenches 220 beneficially allows the doping concentration of at least a portion of the epitaxial layer 204 to be significantly increased, such as, for example, by at least a factor of two in comparison to the doping level of a standard LDMOS device (e.g., about 2×10^{12} to 4×10^{12} atoms per square centimeter, compared to a typical doping concentration of about 1×10^{12} to 2×10^{12} atoms per square centimeter), without an appreciable increase in HCI. In this manner, one or more conventional LDD regions may be omitted, with the epitaxial layer 204 and trenches 220 replacing the function of the LDD regions. Since the epitaxial layer 204 is formed significantly deeper compared to the LDD regions, the current in the LDMOS device can be more easily distributed rather than being concentrated near the silicon/oxide interface, thus contributing to the reduction in HCI effects. Moreover, by increasing the doping concentration of the epitaxial layer, an on-resistance of the device, which is typically a function of the doping level of the LDD region and/or expitaxial layer, is also advantageously reduced. Thus, by forming an MOS device in accordance with the techniques of the present invention, a reduction in on-resistance and HCI effects can be concurrently achieved.

The number and spacing of the trenches 220 relative to one another will be based, at least in part, on the doping concentration of the epitaxial layer 204. In an illustrative embodiment of the invention, the trenches may be spaced from one another at a distance of about two to three microns in an n-type epitaxial layer having a doping concentration on the order of about 10^{16} atoms per cubic centimeter. For a given trench spacing, the number of trenches optimally utilized will depend, at least in part, on the width of the drain region 208. For instance, as the width of the drain region increases, the number of trenches 220 is preferably increased accordingly in order to sustain the same relative benefit.

In a preferred embodiment, at least a portion of the trenches 220 comprises an insulating material 228, such as, for example, an oxide (e.g., silicon dioxide), lining the walls forming the trenches, and an electrically conductive material 230, such as, for example, polysilicon, substantially filling the trenches. The polysilicon material used to fill the trenches is preferably doped with an

impurity (e.g., boron or phosphorous) of a known concentration level so as to form a low-resistance electrical path (e.g., one ohm per square) in the trenches. Although not required, the insulating material 228 lining the walls of the trenches 220 helps control an out-diffusion of the more heavily doped conductive material 230 into the more lightly doped epitaxial layer 204.

5   FIGS. 3A-3D depict steps in an illustrative methodology which may be used in forming the exemplary LDMOS device shown in FIG. 2, in accordance with one embodiment of the present invention. The illustrative methodology will be described in the context of a conventional CMOS-compatible semiconductor fabrication process technology. It is to be understood that the invention is not limited to this or any particular methodology for fabricating the device. Furthermore, as

10   previously stated, the various layers and/or regions shown in the figures may not be drawn to scale and certain commonly used semiconductor layers may have been omitted for ease of explanation.

FIG. 3A depicts a cross section of at least a portion of an exemplary semiconductor wafer 300 in which the techniques of the present invention may be implemented. The wafer 300 includes a substrate 302 and an epitaxial layer 304 formed on the substrate 302. The substrate 302 is

15   preferably a p+ type substrate having a high conductivity, although an n+ type substrate may alternatively be employed. As will be understood by those skilled in the art, a p+ substrate may be formed by adding a p-type impurity or dopant (e.g., boron) of a desired concentration (e.g., about 5×10^{18} to about 5×10^{19} atoms) to the substrate material, such as by a diffusion or implant step, to change the conductivity of the material as desired. The epitaxial layer 304 is then grown over the

20   entire surface of the wafer. The epitaxial layer 304 may also be modified by adding an n-type impurity. A breakdown voltage of the resulting transistor structure is determined, at least in part, by the thickness and impurity concentration of the epitaxial layer 304.

A P-body region 306 is formed in the epitaxial layer 304 such as, for example, by using a deep diffusion or implant step. During the diffusion step, a p-type impurity (e.g., boron) of a known

25   concentration level is preferably used. A gate 308 is formed on an upper surface of an oxide layer 310 in the LDMOS device. The gate 308 may be fabricated from a polycrystalline silicon (polysilicon) layer formed over the thin (e.g., about 300-400 angstroms) oxide layer 310, such as, for example, using a chemical vapor deposition (CVD) technique. The oxide layer 310 under the

gate 308 is often referred to as gate oxide. The polysilicon layer is generally patterned using, for example, a conventional photolithographic process, followed by an etching step (e.g., dry etching) to form gate 308, as will be understood by those skilled in the art. Although not shown, a dummy gate may also be fabricated on the oxide layer 310. The dummy gate, if used, is preferably spaced

5   laterally from the gate 308 in a direction opposite the P-body region 306. Like the gate 308, the dummy gate may comprise polysilicon material.

A source region 312 is formed in the P-body region 306 and a drain region 314 is formed in the epitaxial region 304. The source and drain regions 312, 314 may be formed, for example, by diffusing or implanting an n-type impurity (e.g., arsenic or phosphorous) of a known concentration

10   level into respective regions 306, 304 of the device. The source region 312 preferably uses a peripheral end of the gate 308 to at least partially define the source region, and thus the source region 312 may be considered to be self-aligned with the gate 308.

FIG. 3B illustrates a process of forming openings 316 in the wafer 300 in which conductive trenches will be formed. The openings 316 may be formed by depositing a layer of photoresist (not

15   shown) of the upper surface of the wafer 300 and using a conventional photolithographic patterning step followed by an etching step to remove unwanted portions of the wafer. The openings 316 are preferably formed (e.g., using reactive ion etching (RIE), dry etching, etc.) through the epitaxial layer 304 to expose the substrate 302 as shown.

FIG. 3C depicts a step of forming a layer of oxide 318 over at least sidewalls 317 of the

20   openings 316. The oxide layer 318 may comprise an insulating material such as, but not limited to, silicon dioxide. The oxide layer 318 may be formed of a desired thickness (e.g., about 300-400 angstroms) similar to the gate oxide layer 310 shown in FIG. 3A, for example, using a conventional oxidation process. In an illustrative oxidation process, about 50 angstroms of oxide may be grown, such as by a thermal oxidation step, and about 300 angstroms of oxide may be deposited, such as by

25   a chemical vapor deposition (CVD) step, on at least the sidewalls 317 of the openings 316. A layer of oxide 318 may also be formed on a bottom 319 of the openings 316. As explained above, while the oxide layer 318 coating the sidewalls 317 of the openings 316 is not a requirement of the invention, such oxide layer is preferred in that it provides a barrier to help prevent the out-diffusion

of conductive material (not shown), used to fill the openings, into the epitaxial layer 304 of the wafer 300.

FIG. 3D illustrates a plug formation process. During this process, the oxide layer 318 is substantially removed from at least the bottom portion 319 (see FIG. 3C) of the openings 316, using, for example, a conventional etching step (e.g., an RIE step, dry etching, etc.) to expose the substrate 302 and yet leave the oxide layer 318 on the sidewalls of the openings 316 substantially intact. A conductive material 320, such as, for example, doped polysilicon, metal (e.g., aluminum), etc., is then deposited in the openings 316 so as to substantially fill the openings. The conductive material in the openings 316 forms conductive vias 322 through the epitaxial layer 304 and provide a substantially low-resistance electrical path between the substrate 302 and the upper surface of the wafer 300. The oxide layer 318 substantially lines at least the sidewalls of the conductive vias 322, thereby preventing the conductive material 320 from out-diffusing into the epitaxial layer 304, as previously stated.

Although illustrative embodiments of the present invention have been described herein with reference to the accompanying drawings, it is to be understood that the invention is not limited to those precise embodiments, and that various other changes and modifications may be made therein by one skilled in the art without departing from the scope of the appended claims.

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